What is claimed is:

1. A magnetic random access memory (MRAM) cell, comprising:

an MRAM cell stack located over a substrate; and

first and second write lines spanning opposing termini of the MRAM cell stack;

wherein at least one of the first and second write lines includes at least one first portion spanning the MRAM cell stack and at least one second portion proximate the MRAM cell stack, the first and second portions having first and second cross-sectional areas, respectively, wherein the first cross-sectional area is substantially less than the second cross-sectional area.

2. The MRAM cell of claim 1 wherein the first write line interposes the MRAM cell stack and the substrate and the MRAM cell stack interposes the substrate and the second write line.

3. The MRAM cell of claim 1 wherein the at least one of the first and second write lines includes two second portions proximate opposing sides of the MRAM cell stack.

4. The MRAM cell of claim 1 wherein the first write line includes the first and second portions and the second write line includes at least one third portion spanning the MRAM cell stack and at least one fourth portion proximate the MRAM cell stack, the third and fourth portions having third and fourth cross-sectional areas, respectively, wherein the third cross-sectional area is substantially less than the fourth cross-sectional area.

5. The MRAM cell of claim 1 wherein the first and second portions have first and second thicknesses, respectively, wherein the first thickness is substantially less than the second thickness.

6. The MRAM cell of claim 1 wherein the first thickness ranges between about 1000 Angstroms and about 4000 Angstroms and the second thickness ranges between about 2000 Angstroms and about 6000 Angstroms.

7. The MRAM cell of claim 1 wherein the first and second portions have first and second widths, respectively, wherein the first width is substantially less than the second width.

8. The MRAM cell of claim 7 wherein the first width ranges between about 500 Angstroms and about 5000 Angstroms and the second width ranges between about 1000 Angstroms and about 10,000 Angstroms.

9. The MRAM cell of claim 1 wherein:

the first and second portions have first and second thicknesses, respectively, wherein the first thickness is substantially less than the second thickness; and

the first and second portions have first and second widths, respectively, wherein the first width is substantially less than the second width.

10. The MRAM cell of claim 1 wherein the first cross-sectional area is at least about 20% less than the second cross-sectional area.

11. The MRAM cell of claim 1 wherein the first write line is a memory array word line and the second write line is a memory array bit line.

12. The MRAM cell of claim 1 further comprising a cladding layer at least partially surrounding the first portion.

13. The MRAM cell of claim 12 wherein at least a portion of a profile of the cladding layer is substantially similar to at least a portion of a profile of the second portion.

14. The MRAM cell of claim 1 further comprising a cladding layer at least partially surrounding each of the first and second portions.

15. A magnetic random access memory (MRAM) cell, comprising:

an MRAM cell stack located over a substrate;

a first write line opposite the MRAM cell stack from the substrate and including a first portion and at least two second portions, the first portion spanning the MRAM cell stack and having a first cross-sectional area, the second portions located proximate opposing sides of the MRAM cell stack and having second cross-sectional areas each substantially greater than the first cross-sectional area; and

a second write line interposing the MRAM cell stack and the substrate and including a third portion and at least two fourth portions, the third portion spanning the MRAM cell stack and having a third cross-sectional area, the fourth portions located proximate opposing sides of the MRAM cell stack and having fourth cross-sectional areas each substantially greater than the third cross-sectional area.

16. The MRAM cell of claim 15 wherein the first and second portions have first and second thicknesses, respectively, wherein the first thickness is substantially less than the second thickness.

17. The MRAM cell of claim 15 wherein the first and second portions have first and second widths, respectively, wherein the first width is substantially less than the second width.

18. The MRAM cell of claim 15 wherein:

the first and second portions have first and second thicknesses, respectively, wherein the first thickness is substantially less than the second thickness; and

the first and second portions have first and second widths, respectively, wherein the first width is substantially less than the second width.

19. The MRAM cell of claim 15 further comprising:

a first cladding layer at least partially surrounding the first portion, wherein first cladding layer has a profile substantially similar to a profile of the second portions; and

a second cladding layer at least partially surrounding the third portion, wherein the third cladding layer has a profile substantially similar to a profile of the fourth portions.

20. The MRAM cell of claim 15 further comprising a first cladding layer at least partially surrounding the first portion and a second cladding layer at least partially surrounding the third portion.

21. The MRAM cell of claim 15 further comprising a first cladding layer at least partially surrounding each of the first and second portions and a second cladding layer at least partially surrounding each of the third and fourth portions.

22. A method of manufacturing a magnetic random access memory (MRAM) cell, comprising:

forming an MRAM cell stack located over a substrate; and

forming first and second write lines spanning opposing termini of the MRAM cell stack;

wherein at least one of the first and second write lines includes at least one first portion spanning the MRAM cell stack and at least one second portion proximate the MRAM cell stack, the first and second portions having first and second cross-sectional areas, respectively, wherein the first cross-sectional area is substantially less than the second cross-sectional area.

23. The method of claim 22 wherein the at least one of the first and second write lines includes two second portions proximate opposing sides of the MRAM cell stack.

24. The method of claim 22 wherein the first write line includes the first and second portions and the second write line includes at least one third portion spanning the MRAM cell stack and at least one fourth portion proximate the MRAM cell stack, the third and fourth portions having third and fourth cross-sectional areas, respectively, wherein the third cross-sectional area is substantially less than the fourth cross-sectional area.

25. The method of claim 22 wherein the first and second portions have first and second thicknesses, respectively, wherein the first thickness is substantially less than the second thickness.

26. The method of claim 22 wherein the first and second portions have first and second widths, respectively, wherein the first width is substantially less than the second width.

27. The method of claim 22 wherein:

the first and second portions have first and second thicknesses, respectively, wherein the first thickness is substantially less than the second thickness; and

the first and second portions have first and second widths, respectively, wherein the first width is substantially less than the second width.

28. The method of claim 22 further comprising forming a cladding layer at least partially surrounding the first portion.

29. The method of claim 28 wherein at least a portion of a profile of the cladding layer is substantially similar to at least a portion of a profile of the second portion.

30. The method of claim 22 further comprising forming a cladding layer at least partially surrounding each of the first and second portions.

31. An integrated circuit device, comprising:

a magnetic random access memory (MRAM) cell located over a substrate, the MRAM cell including:

an MRAM cell stack located over the substrate; and

first and second write lines spanning opposing termini of the MRAM cell stack;

wherein at least one of the first and second write lines includes at least one first portion spanning the MRAM cell stack and at least one second portion proximate the MRAM cell stack, the first and second portions having first and second cross-sectional areas, respectively, wherein the first cross-sectional area is substantially less than the second cross-sectional area;

a transistor device formed at least partially in the substrate; and

an interconnect coupling one of the first and second write lines and the transistor device.

32. The integrated circuit device of claim 31 wherein the at least one of the first and second write lines includes two second portions proximate opposing sides of the MRAM cell stack.

33. The integrated circuit device of claim 31 wherein the first write line includes the first and second portions and the second write line includes at least one third portion spanning the MRAM cell stack and at least one fourth portion proximate the MRAM cell stack, the third and fourth portions having third and fourth cross-sectional areas, respectively, wherein the third cross-sectional area is substantially less than the fourth cross-sectional area.

34. The integrated circuit device of claim 31 wherein the first and second portions have first and second thicknesses, respectively, wherein the first thickness is substantially less than the second thickness.

35. The integrated circuit device of claim 31 wherein the first and second portions have first and second widths, respectively, wherein the first width is substantially less than the second width.

36. The integrated circuit device of claim 31 wherein:

the first and second portions have first and second thicknesses, respectively, wherein the first thickness is substantially less than the second thickness; and

the first and second portions have first and second widths, respectively, wherein the first width is substantially less than the second width.

37. The integrated circuit device of claim 31 further comprising forming a cladding layer at least partially surrounding the first portion.

38. The integrated circuit device of claim 37 wherein at least a portion of a profile of the cladding layer is substantially similar to at least a portion of a profile of the second portion.

39. The integrated circuit device of claim 31 further comprising forming a cladding layer at least partially surrounding each of the first and second portions.